BIASING CIRCUIT AND VOLTAGE CONTROL OSCILLATOR THEREOF

DESCRIPTION

CROSS-REFERENCE TO RELATED APPLICATION

[Para 1] This application claims the priority benefit of Taiwan application serial no. 93121259, filed July 16, 2004.

BACKGROUND OF INVENTION

[Para 2] Field of the Invention

[Para 3] The present invention relates to a biasing circuit, and more particularly to a biasing circuit with a compensation circuit for stabilizing the output thereof.

[Para 4] Description of Related Art

[Para 5] Phase Lock Loop (PLL) has been widely used in the design of integrated circuits, especially in frequency combination, clock feedback and data feedback. The key element in the PLL is Voltage Control Oscillator (VCO) and the VCO directly affects the performance of the PLL.

[Para 6] FIG. 5 is a circuit block diagram showing a prior art VCO. Referring to FIG. 5, the VCO 500 comprises a replica biasing circuit 502, a voltage/current converter 504, a ring oscillator 508, a differential circuit 510 and a reference voltage generating circuit 532.

[Para 7] FIG. 6 is a schematic drawing showing a prior art VCO. The biasing circuit 502 comprises a comparison circuit 516 and a delay circuit 514. The delay circuit 514 comprises a variable current source 522, a first transistor M51, a first resistor circuit 524, a second transistor M52 and a second resistor

circuit 526. The variable current source 522 receives the input current and an operational voltage, and outputs a variable current from a current output terminal of the variable current source 522. The first transistor M51 comprises a drain terminal, a source terminal and a gate terminal, wherein the source terminal is coupled to the current output terminal of the variable current source 522, the gate terminal is grounded and the drain terminal is coupled to the first resistor circuit 524. The first resistor circuit 524 comprises a first terminal, a second terminal and a third terminal, wherein the second terminal is grounded and the third terminal is coupled to the output terminal of the comparison circuit 516. The resistance of the first resistor circuit 524 varies with the comparison signal.

[Para 8] The second transistor M52 comprises a source terminal, a drain terminal and a gate terminal, wherein the source terminal is coupled to the current output terminal of the variable current source 522 and the gate terminal is coupled to the third input terminal of the delay circuit 544, i.e. the reference voltage. The second resistor circuit 526 comprises a first terminal, a second terminal and a third terminal, wherein the first terminal is coupled to the drain terminal of the second transistor M52, the second terminal is grounded and the third terminal is coupled to the output terminal of the comparison circuit 516. The resistance of the first resistor circuit 126 varies with the comparison signal.

[Para 9] The first output terminal of the delay circuit 514 is disposed between the first transistor M51 and the first resistor circuit 524, and the second output terminal of the delay circuit 514 is disposed between the second transistor M52 and the second resistor circuit 526.

[Para 10] In the prior art technology, the voltage/current converter 504 receives and converts the input voltage into an input current. The voltage/current converter 504 outputs the input current to the replica biasing circuit 502 and the ring oscillator 508. The replica biasing circuit 502 generates the first differential voltage and the second differential voltage according to the reference voltage output from the reference voltage generating circuit 532 and the current provided by the variable current source

522. The comparison circuit 516 outputs the comparison signal to the first resistor circuit 524 and the second resistor circuit 526 according to the reference voltage and the first differential voltage. The delay circuit 514 provides the second differential voltage to the ring oscillator 508. The ring oscillator 508 and the differential circuit 510 output the clock signal according to the input current, the first differential voltage and the second differential voltage.

[Para 11] FIGS. 7A and 7B are small-signal analysis curves of the prior art replica biasing circuit. The DC gain is equal to 71.36 dB. The whole frequency bandwidth of the gain is about 4.06 MHz, and the phase margin is about 37 degrees. The first-port frequency is about 2.06 kHz, and the second-port frequency is about 2.83 MHz.

[Para 12] FIGS. 7A and 7B show the voltage-gain/frequency curves of the prior art PLL. FIG. 7A represents the input voltage curve at the input terminal of the voltage control oscillator 500. FIG. 7B represents the output at the port 523 of the replica biasing voltage 514. According to the curve in FIG. 7B, when the variable current source 522 provides small currents, an output jitter at port 523 is generated.

[Para 13] Accordingly, as the replica biasing circuit 514 cannot stabilize the output thereof under low-current or low-frequency operations, the output jitter of the voltage control oscillator 500 occurs.

SUMMARY OF THE INVENTION

[Para 14] Accordingly, the present invention is directed to a biasing circuit comprising a compensation circuit capable of stabilizing the output current regardless of high or low output currents from the biasing circuit.

[Para 15] The present invention is also directed to a voltage control oscillator. By using a compensation circuit in the biasing circuit, the jitter of the clock frequency output from the voltage control oscillator can be suppressed.

[Para 16] The present invention discloses a biasing circuit for receiving the input current and the reference voltage. The biasing circuit comprises a delay

circuit, a compensation circuit and a comparison circuit. The delay circuit comprises a first input terminal, a second input terminal, a third input terminal and a fourth input terminal, and a first output terminal and a second output terminal, wherein the first input terminal receives the input current, the second input terminal is grounded and the third input terminal receives the reference voltage. The compensation circuit is coupled to the first output terminal of the delay circuit and outputs a compensation voltage according to a first differential voltage at the first output terminal of the delay circuit. The comparison circuit comprises a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is coupled between the compensation circuit and the first output terminal of the delay circuit so as to receive the compensation voltage and the second output terminal receives the reference voltage. The comparison circuit is adapted for comparing the compensation voltage and the reference voltage to output a comparison signal from the output terminal of the comparison circuit to the fourth input terminal of the delay circuit, wherein the delay circuit outputs a second differential voltage from the second output terminal of the delay circuit according to the input current and the comparison signal.

[Para 17] According to an embodiment of the present invention, the compensation circuit comprises a constant current source and a voltage detecting circuit. The constant current source comprises a first terminal and a second terminal, wherein the second terminal outputs a constant current. The voltage detecting circuit is coupled to the second terminal of the constant current source and generates the compensation voltage according to the constant current. The second output terminal of the delay circuit is coupled between the constant current source and the voltage detecting circuit.

[Para 18] The present invention also discloses a voltage control oscillator for receiving an input current and a reference voltage. The voltage control oscillator comprises a voltage/current converter, a biasing circuit and an oscillation circuit. The voltage/current converter receives and converts the input voltage into an input current. The voltage/current converter outputs the input current. The biasing circuit comprises a delay circuit, a compensation

circuit and a comparison circuit. The biasing circuit outputs a first differential voltage and a second differential voltage according to the input current and the reference voltage. The oscillation circuit is coupled to the voltage/current converter and the biasing circuit for receiving the input current, the first differential voltage and the second differential voltage and outputting a clock signal according thereto.

[Para 19] The present invention also discloses an electronic device comprising at least one biasing circuit. The biasing circuit comprises a delay circuit, a compensation circuit and a comparison circuit. The delay circuit comprises a first input terminal, a second input terminal, a third input terminal and a fourth input terminal, and a first output terminal and a second output terminal, wherein the first input terminal receives the input current, the second input terminal is grounded and the third input terminal receives the reference voltage. The compensation circuit is coupled to the first output terminal of the delay circuit and outputs a compensation voltage according to a first differential voltage at the first output terminal of the delay circuit. The comparison circuit comprises a first input terminal, a second input terminal and an output terminal. The first input terminal of the comparison circuit is coupled between the compensation circuit and the first output terminal of the delay circuit so as to receive the compensation voltage. The second output terminal of the comparison circuit receives the reference voltage. The comparison circuit compares the compensation voltage and the reference voltage so as to output a comparison signal from the output terminal of the comparison circuit to the fourth input terminal of the delay circuit. The delay circuit outputs a second differential voltage from the second output terminal of the delay circuit according to the input current and the comparison signal.

[Para 20] The present invention discloses another electronic device comprising at least one voltage control oscillator. The voltage control oscillator circuit receives an input voltage and a reference voltage. The voltage control oscillator comprises a voltage/current converter, a biasing circuit and an oscillation circuit. The voltage/current converter outputs the input current. The biasing circuit comprises a delay circuit, a compensation circuit and a

comparison circuit. The biasing circuit outputs a first differential voltage and a second differential voltage according to the input current and the reference voltage. The oscillation circuit is coupled to the voltage/current converter and the biasing circuit for receiving the input current, the first differential voltage and the second differential voltage and outputs a clock signal according to the input current, the first differential voltage and the second differential voltage.

[Para 21] According to an embodiment of the present invention, the compensation circuit disposed in the biasing circuit. When the biasing circuit is operating under small current or small frequency, the biasing circuit suppresses the jitter of the output clock frequency of the voltage control oscillator.

[Para 22] The above and other features of the present invention will be better understood from the following detailed description of the preferred embodiments of the invention that is provided in communication with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[Para 23] FIG. 1 is a circuit block diagram showing a voltage control oscillator according to an embodiment of the present invention.

[Para 24] FIG. 2 is a schematic drawing showing a compensation circuit according to an embodiment of the present invention.

[Para 25] FIGS. 3A-3B and 4A-4B are a small-signal analysis curve of a compensation circuit, an input voltage curve of a voltage control oscillator, a first differential voltage curve and a second differential voltage curve according to an embodiment of the present invention.

[Para 26] FIG. 5 is a circuit block diagram showing a prior art VCO.

[Para 27] FIG. 6 is a schematic drawing showing a prior art VCO.

[Para 28] FIGS. 7A and 7B are small-signal analysis curves of the prior art replica biasing circuit.

[Para 29] FIGS. 8A is a conventional input voltage curve of a voltage control oscillator.

[Para 30] FIGS. 8B is a conventional first differential voltage curve and a second differential voltage curve.

DESCRIPTION OF EMBODIMENTS

[Para 31] FIG. 1 is a circuit block diagram showing a voltage control oscillator according to an embodiment of the present invention. The voltage control oscillator 100 comprises a biasing circuit 102, a voltage/current converter 104, an oscillation circuit 106 and a reference voltage generating circuit 132. One of ordinary skill in the art will understand that the biasing circuit 102 can be, for example, a replica biasing circuit, but not limited thereto.

[Para 32] In this embodiment, the voltage/current converter 104 receives and converts the input voltage into an input current. The voltage/current converter 104 outputs the input current to the biasing circuit 102 and the oscillation circuit 106. The biasing circuit 102 is coupled to the voltage/current converter 104 having a delay circuit 112, a compensation circuit 114 and a comparison circuit 116. The delay circuit 114 comprises a first input terminal, a second input terminal, a third input terminal and a fourth input terminal, and a first output terminal and a second output terminal, wherein the first input terminal receives the input current, the second input terminal is grounded and the third input terminal of the delay circuit 114 receives the reference voltage output from the reference voltage generating circuit 132.

[Para 33] The compensation circuit 112 is coupled to the first output terminal of the delay circuit 114 and outputs a compensation voltage according to a first differential voltage at the first output terminal of the delay circuit 114. FIG. 2 is a schematic drawing showing a compensation circuit according to an embodiment of the present invention. Referring to FIG. 2, the compensation circuit 112 may comprise, for example, the constant current source 202 and the voltage detecting circuit 204. The constant current source 202 comprises a first terminal and a second terminal, wherein the second terminal outputs a

constant current to the voltage detecting circuit 204. The voltage detecting circuit 204 generates the compensation voltage according to the constant current. The second output terminal of the delay circuit 114 is coupled between the constant current source 202 and the voltage detecting circuit 204.

[Para 34] The voltage detecting circuit 204 can be, for example, a resistor, but not limited thereto.

[Para 35] Referring to FIG. 1, the comparison circuit 116 comprises a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is coupled between the compensation circuit 112 and the first output terminal of the delay circuit 114 so as to receive the compensation voltage and the second output terminal receives the reference voltage. The comparison circuit 116 compares the compensation voltage and the reference voltage to output a comparison signal from the output terminal of the comparison circuit 116 to the fourth input terminal of the delay circuit 114, wherein the delay circuit 114 outputs a second differential voltage from the second output terminal of the delay circuit 114 to the oscillation circuit 106 according to the input current and the comparison signal.

[Para 36] In the present embodiment, the oscillation circuit 106 is coupled to the voltage/current converter 104 and the biasing circuit 102 for receiving the input current, the first and second differential voltages, and outputting a clock signal according thereto.

[Para 37] In the present embodiment, the delay circuit 114 comprises a variable current source 122, a first transistor M1, a first resistor circuit 124, a second transistor M2 and a second resistor circuit 126. The variable current source 122 receives the input current and an operational voltage. The variable current source 122 outputs a variable current from a current output terminal of the variable current source 122. The first transistor M1 comprises a drain terminal, a source terminal and a gate terminal, wherein the source terminal is coupled to the current output terminal of the variable current source 122 and the gate terminal is grounded. The drain terminal of the first transistor M1 is coupled to the first resistor circuit 124. The first resistor circuit 124 comprises a first terminal, a second terminal and a third terminal. The second

terminal of the first resistor circuit 124 is grounded, and the third terminal of the first resistor circuit 124 is coupled to the output terminal of the comparison circuit 116. The resistance of the first resistor circuit 124 varies with the comparison signal.

[Para 38] In this embodiment, the second transistor M2 comprises a source terminal, a drain terminal and a gate terminal, wherein the source terminal is coupled to the current output terminal of the variable current source 122 and the gate terminal is coupled to the third input terminal of the delay circuit 144, i.e. the reference voltage. The second resistor circuit 126 comprises a first terminal, a second terminal and a third terminal, wherein the first terminal is coupled to the drain terminal of the second transistor M2, the second terminal is grounded and the third terminal is coupled to the output terminal of the comparison circuit 116. The resistance of the first resistor circuit 126 varies with the comparison signal.

[Para 39] The first output terminal of the delay circuit 114 is disposed between the first transistor M1 and the first resistor circuit 124, and the second output terminal of the delay circuit 114 is disposed between the second transistor M2 and the second resistor circuit 126.

[Para 40] In the present embodiment, the first resistor circuit 124 may comprise, for example, one or more transistors. The second resistor circuit 126 may also comprise, for example, one or more transistors. The present invention, however, is not limited thereto.

[Para 41] In the present embodiment, the oscillation circuit 106 may comprise, for example, a ring oscillator 108 and a differential circuit 110. In the oscillation circuit 106, the gate terminal of the second transistor M2 of the first-level delay circuit is coupled to the second output terminal of the delay circuit 114. The ring oscillation circuit 108 may comprise a plurality of delay circuits. But the invention is not limited thereto.

[Para 42] In the present embodiment, the reference voltage can be generated, for example, by a reference voltage generating circuit 132.

[Para 43] Referring to FIGS. 1 and 2, the voltage control oscillator 100 converts the input voltage into an input current and outputs the input current to the delay circuit 114 and the ring oscillator 106. The delay circuit 114 provides currents to the first transistor M1 and the second transistor M2. A first differential voltage is at the first output terminal, P2, of the delay circuit 114. The compensation circuit 112 outputs the compensation voltage to the first input terminal of the comparison circuit 116 according to the first differential voltage.

[Para 44] The comparison circuit 116 compares the reference voltage and the compensation voltage and outputs the comparison signal to the first resistor circuit 124 and the second resistor circuit 126. The delay circuit 114 outputs the first compensated differential voltage and the second compensated differential voltage to the oscillation circuit 106 and the oscillation circuit 106 outputs the clock signal.

[Para 45] In the present embodiment, a small-signal ac analysis method is used to analyze the output stability of the biasing circuit. A two-port model, P1 and P2, is used to analyze the replica biasing circuit. If the high-level port is disregarded, the capacitance is C_{23}, the output impedance of the operational amplifier is r_{op} at the first port P1, and the port frequency $\omega_1 = 1 / r_{op}C_{23}$. The second port P2 relates to the feedback port N1 and the port frequency $\omega_2 = 1/R_2C_{N1}$, wherein is the capacitance at the port N1. The equivalent resistance R_2 is $(r_{122}+r_{M1}) \parallel r_{124} \parallel R_{204} \parallel r_{202}$. Because the output impedances of the variable current source 122 and the constant current source 141 are higher than the others, the equivalent resistance R_2 becomes $r_{124} \parallel R_{204}$.

[Para 46] In the present embodiment, the voltage detecting circuit 204 controls the equivalent impedance at the second port. Accordingly, the maximum impedance R_{2max} at the second port P2 is substantially equivalent to the impedance R_{204}. The minimum frequency ω_2 at the second port P2 is fixed as $1/R_{204}C_{31}$. The compensation resistor 204 affects the dc biasing port. The affection can be removed by using the constant current source 202 in the

compensation circuit 112. The constant current output from the constant current source 202 is equivalent to reference voltage/ R_{204}.

[Para 47] FIGS. 3A-3B and 4A-4B are a small-signal analysis curve of a compensation circuit, an input voltage curve of a voltage control oscillator, a first differential voltage curve and a second differential voltage curve according to an embodiment of the present invention.

[Para 48] Referring to FIGS. 3A and 3B, the DC gain is equal to 61.7 dB. The whole frequency bandwidth of the gain is about 2.36 MHz, and the phase margin is about 73 degrees. The first-port frequency is about 2.06 kHz, and the second-port frequency is about 9.75 MHz. The first-port frequency of the present invention is similar to that without the compensation circuit. By adding the compensation circuit, the phase margin increases from 37 degrees to 73 degrees.

[Para 49] FIGS. 4A and 4B show the curves of a phase lock loop with the compensation circuit. FIG. 4A represents the input voltage curve at the input terminal of the voltage control oscillator 100. FIG. 4B represents the output at the port 23 of the biasing voltage 114. These curves show the output of the biasing circuit is stable.

[Para 50] Accordingly, the biasing circuit and the voltage control oscillator thereof stabilizes the output of the biasing circuit while the biasing circuit is being operated by low currents or low frequencies. Thus, the jitter of the output clock signal of the voltage control oscillator can be suppressed.

[Para 51] Although the present invention has been described in terms of exemplary embodiments, it is not limited thereto. Rather, the appended claims should be constructed broadly to include other variants and embodiments of the invention, which may be made by those skilled in the field of this art without departing from the scope and range of equivalents of the invention.